THE USE OF MICROPROCESSORS AT TRIUMF IN THE CONTROL OF RADIATION SAFETY INTERLOCK SYSTEMS

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ABSTRACT

At TRIUMF the cyclotron vault, all primary beam lines, and each experimental area has a dedicated control unit to manage the safety interlock control of the area lockup sequence, beam blocker drive and area access. Typically each area has 24 devices which are monitored to control 16 outputs. These control units (Area Safety Units) were first implemented through the use of relay logic. The relay logic was reliable but difficult to modify to incorporate changes to the areas. In 1979 it was decided to use microprocessors in the form of single board computers to control the Area Safety Units. This paper will discuss the details of the hardware and software used as well as the advantages of microprocessor control.

INTRODUCTION

The TRIUMF cyclotron is capable of accelerating H^- ions to an energy greater than 500 MeV at currents exceeding 100 microamperes. This results in radiation fields greater than 1 Gray per hour in certain areas which dictates that personnel must be excluded from these areas during operation. To accomplish this there is an extensive safety interlock system comprised of the Central Safety System (CSS)[1] for global site radiation safety and machine protect, and dedicated Area Safety Units for control of the exclusion areas.

At present there are 12 such personnel exclusion areas. The ASU controls the area lockup sequence and may also provide control over local devices such as beam blockers or radiation emission devices such as RF or DC separators. Each ASU operates independently and makes decisions based on the status of local devices and signals received from the CSS. The results are then sent to the CSS or used to control local devices. Signals are sent from the CSS to the ASU to enable the operation of certain local devices.

TYPICAL LOCKUP AREA

Each area's safety system consists of an exclusion area (walls, fences, etc.), doors, a lockup chain, alarms (horns and beacons) and an ASU. In addition to these devices there must be at least 2 or 3 devices to prevent beam from being delivered to the areas. The lockup chain ensures that a physical search of the area is completed before beam can be delivered to the area. Depending on the physical layout of the area, the lockup sequence may require one or two people to complete.

A lockup chain consists of a series of watchman stations which are connected in such a manner that they have to be armed in a specific sequence. The watchman stations have a push-button to "arm" and an emergency trip push-button or "Panic Button" which is hardwired directly to a fast trip relay circuit. The watchman stations are physically positioned so that the entire area must be checked to complete the sequence.

The door lock mechanism is such that the gate or door must be closed and locked before the key can be removed. Where there is more than one door a transfer lock is included in the lockup routine. The transfer lock mechanism has a tumbler for each door in the area and includes a control key. All the keys from the doors must be inserted and turned in the transfer lock before the control key can be removed and the control key has

to be inserted and turned before any of the other keys can be removed. Either the control key, or if there is only one door, the door key must be inserted and turned to the capture position in the key release unit as one of the conditions to define the area as "secured". Microswitches signal the ASU logic when the key is captured in the release unit and the release of the keys is controlled by the ASU. This method of keying ensures that all doors must be closed and locked during the operation of an area.

MICROPROCESSOR CONTROLLED AREA SAFETY UNITS

When the decision was made to change from relay logic to microprocessors for the control of the ASUs there were a few conditions that had to be met.

1 The program had to be stored in EPROM

2 The system had to be able to self start on a powerup

3 Must use high true logic(+24 VDC for a true or "on" condition).

4 The Central Safety System employs Boolean algebra using standard logic notation ("*" is the AND function, "+" is the "OR" function,etc.) to determine which outputs to set to a true condition. It was desirable to retain the Boolean algebra capabilities in any new design.

The first microprocessor controlled ASUs used a single board computer (SBC) manufactured by Cromemco. The board was Z80 based, had 4 I/O ports, 1 serial and 3 parallel, and included sockets for four 2716 EPROMs. Two of the sockets were populated with EPROMs which contained Control Basic and a monitor program. The Control Basic is an interpreter basic which handles boolean algebra utilizing standard logic notation. Industry standard opto-isolated I/O modules and mounting racks were interfaced to the processor board via a fan-out board and associated cabling. After the program was debugged it was burned into EPROMs which were then installed in the sockets on the SBC. The system would autostart on a reset or powerup.

THE STD BUS

A major component on the single board computer was obsoleted by the integrated circuit manufacturer which rendered the boards impractical for any future designs. It was therefore necessary to select a new system to install in future designs using the same criteria as in the original selection with the additions that:

1 The equipment must be multi-sourced

2 The new equipment must maintain as much compatibility as possible with existing equipment.

For these reasons the STD BUS was chosen. I/O boards are manufactured for the STD BUS which connect directly to the existing module mounting racks through a 50 conductor ribbon cable. These boards are industry standard and are produced by a number of different companies. A wide range of microprocessor boards is also readily available including one which has an EPROM based basic that supports all the instructions included in the Cromemco version with some enhancements. By selecting the STD BUS any future upgrades can be implemented merely by replacing boards in the STD BUS card cage

without any changes to the field wiring. To upgrade the existing microprocessor controlled ASUs to the STD-BUS the single board computer and fan out board are removed and replaced by a card cage, associated boards and a power supply.

AREA SAFETY UNIT HARDWARE (Details)

Input Output Section

External input signal levels are at +24 VDC for a true or safe condition and all devices driven by the ASU must receive +24 VDC or 115 VAC to operate. The +24 VDC and 115 VAC power is supplied by an uninterruptable power supply. Any interruption or break in the cabling to or from the ASU will disable the appropriate devices and fail safe. Plug in modules as per Nema ICS 2-230.02 are used to convert these levels to +5 logic levels for the STD rack. The modules incorporate opto-isolators to provide 2500 VAC isolation between the field wiring and the logic levels for both input and output modules. Racks are available to house 4, 8, 16, or 24 modules and have a separate LED indicator and fuse, between module and external circuitry, for each module. The I/O module mounting racks are connected to the General Purpose Interface Card (I/O board) in the STD BUS via edge connectors and a 50 conductor ribbon cable. Each I/O board can interface to 24 or 48 inputs and/or outputs and require 4 or 8 consecutive port addresses which are set by onboard plug in jumpers. All components in the I/O section are multi-sourced and are readily available.

Microprocessor

A number of processor boards are manufactured for the STD BUS incorporating all of the major microprocessor chips. The board selected for the first STD BUS installations was a Z80 based board with 2 RS-232 serial ports, 4 byte wide memory sockets and a basic interpreter on EPROM. Onboard jumpers are used to configure the sockets for size and type of memory RAM, EPROM or EEPROM. In the development system, EPROM based BASIC firmware occupies one socket, two sockets contain RAM and the forth socket contains an EEPROM. In the operating system the EEPROM is replaced by an EPROM.

ASU SOFTWARE

An ASU program consists of five main areas:

1 initialization; all variables are set to zero

2 variable assignments; the input ports are read and the value is assigned to an array variable. Array variables conserve the limited number of integer variables supported by BWS-Basic. BWS-Basic supports 52 integer variables referenced as A-Z and A0-Z0. Each bit in these arrays is extracted and declared as a integer variable.

3 This section contains the Boolean algebra equations which determine the status of the outputs. The first two lines of this section constitute a watchdog timer routine which toggles the first output module once every cycle through the program

4 In this portion, input latch and timer functions are executed. Input latches are necessary to hold a value for a momentary contact device such as a push-button or door microswitch. The length of time the lockup alarm sounds and the time allocated to complete the lockup sequence are examples of timer functions performed by the ASU. The timers do not use the timer functions incorporated in BWS-Basic as the software overhead required by this function would result in unacceptably long program cycle times. Rather, array variables are set to a numeric value and these are decremented each cycle to a zero value at which point the timed task halts.

5 Here the output variable bits are packed into 8 bit bytes and sent to the output ports. The final line of the program is a statement to return program execution to the start of section #2.

In the change over to the STD BUS BWS-BASIC is employed to implement the logic. The advantage of Basic is that it is readily understood and although the syntax varies from one "BASIC" to another the underlying structure remains the same. When upgrading one the earlier SBC controlled ASUs to the STD BUS the syntax of some of the routines had to be rewritten but the Boolean equations did not change. This meant that once the initialization, input, variable assignment, and output routines had been written the equations could be imported from the SBC version.

The program for the STD-BUS was written on an IBM PC/XT clone using a memory resident program incorporating a full screen editor. The program was written and saved on the PC and then transfered to the STD-BUS using a terminal emulator program that provides ASCII file transfer and capture.

Once the program is transferred to the STD BUS it is tested on a simulator which consists of all of the hardware of an operational ASU but employs switches to simulate inputs and LEDs to display the status of the outputs. During the debugging process changes to the program for diagnostic purposes are written to the STD-BUS CPU RAM while changes to the program are done on the PC and transferred to the STD-BUS. This is to ensure that there is a record of program changes.

The next phase is implemented once the program appears to have all the bugs removed and involves moving the program from RAM to a semi-permanent memory either a battery backed RAM or an EEPROM. This is necessary to check that the program will perform properly on a power up or reset. The program is then thoroughly checked using the simulator.

The development system is now ready for long term testing which involves setting up the simulator to mimic the operating modes of the lockup area it will be installed in. It is run in each mode for a number of days to try and induce a failure. If the program passes this test it is transferred to an EPROM which is then installed on the CPU board. The long term tests are again run and when these are passed the CPU board is ready to install in an ASU. The first STD BUS controlled ASU was installed in the Spring of 1987. There is a TRIUMF Safety Group document available with further details on both the hardware and software for this system.

The major advantages of the microprocessor installations are that any changes to the operating modes of an experimental area generally only necessitate modifications to the software. Previously, any modifications to the relay logic often required major rewiring. There was no simulator available for the relay logic ASUs. This meant that the major testing had to be done after the changes were implemented. Both the modification and testing involved considerable time. This made for very inflexible systems. With the use of microprocessors all the changes and major testing could be done prior to installing the CPU board in the ASU. The use of the microprocessor has resulted in more flexible and reliable safety interlocks for experimental areas.

References

1) J. Drozdoff, et al. The Safety Interlock System At TRIUMF
International Radiation Protection Association 6th International Congress Proceedings.